Abstract

A circuit is provided with a plurality of interconnected logic blocks, a main clock generator for distributing a reference clock signal to the logic blocks. Each logic block in the circuit comprises a local clock generator that generates a set of synchronized local clock signals from the reference clock signal for further provision to respective elements of the logic block. In such a circuit, a phase shift is introduced between a set of local clock signals of a first block and a set of local clock signals of a second block.